Accelerating Particle Image Velocimetry with FPGAs
NORTHEASTERN UNIVERSITY
ECE DEPARTMENT
Abderrahmane Bennis, Miriam Leeser, Gilead Tadmor, Russ Tedrake
abeennis@ece.neu.edu                              mel@ece.neu.edu                  tadmor@ece.neu.edu               Russt@mit.edu

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Goal
Accelerate the performance of highly parameterized Particle Image Velocimetry (PIV) algorithm using Field Programmable Gate Arrays (FPGAs)

Abstract
Particle image velocimetry (PIV) is used in computational fluid dynamics to obtain a detailed localized view of velocity vectors in an unsteady fluid flow. In a nutshell, the estimated velocity field is computed from local correlations of snapshot-pairs of the particle-seeded flow, obtained by high-speed cameras. PIV is used to study aerodynamics of birds and planes, among other applications. Techniques to implement PIV make use of optics, fluid mechanics, imaging techniques and computing. In different engineering applications, different PIV parameters are required. For instance, in control applications, PIV might be used only when real-time response is possible. Up to now, there is no PIV system that combines both, flexible parameterization and high computing performance. In our research we are creating such a system.

We have designed a highly parameterized PIV implementation based on reconfigurable hardware that adapts to various setups and application domains. The circuit is parameterized by the dimensions of the captured images as well as the dimensions of the interrogation windows and sub-areas, pixel representation, board memory width, displacement and overlap. Through this work a parameterized library of different VHDL components has been built. For a typical PIV configuration with images of $512 \times 512$ pixels, $40 \times 40$ pixel interrogation windows and $32 \times 32$ pixel sub-areas, we achieved about 65x speedup in hardware over a standard software implementation. This research is supported by the National Science Foundation.

Contributions
- A highly parameterized digital PIV system is designed using VHDL.
- A highly parameterized digital PIV is implemented on a FPGA board
- A library of parameterized VHDL components has been built
- C++ implementation of parameterized PIV

References:

ADM-XRC-5LX Board Block Diagram

Speedup of Different Circuits

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Hardware latency (sec)</th>
<th>Software latency (sec)</th>
<th>Speedup</th>
</tr>
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<tbody>
<tr>
<td>C1</td>
<td>0.003</td>
<td>0.17</td>
<td>56</td>
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<tr>
<td>C2</td>
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<td>5.04</td>
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Our design outperforms [1], last advanced circuit, by processing 333 pairs of images per second instead of 204.

Future Work
Look at ways to optimize the performance of the design by:
- Duplicate the correlator unit
- Insert more parallelism in the design
- Add Sub-pixel interpolation option to the design
- work with the Robot Locomotion Group at MIT [2] to integrate the circuit in a Feedback loop to control standing up a wing

http://www.alpha-data.com/adm-xrc-5lx.html