Implementation of a Highly Parameterized Digital PIV System On Reconfigurable Hardware

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Algorithm

Goal

Measurement of the wake vortices of a lifting aircraft wing

Accelerate the performance of a highly parameterized Particle Image Velocimetry (PIV) algorithm using Cross-correlation

Abstract

Particle image velocimetry (PIV) is used in computational fluid dynamics to obtain a detailed localized view of velocity vectors in an unsteady fluid flow. The estimated velocity field is computed from local correlations of snapshot pairs of the particle-seeded flow, obtained by high-speed cameras. Despite many improvements to PIV methods over the last twenty years, PIV post-processing remains a computationally intensive task. It becomes a serious bottleneck as snapshot acquisition rates reach O(10kHz). In this research we aim to substantially speed up PIV post-processing by implementing it in reconfigurable hardware. This implementation is highly parameterized, supporting adaptation to varying setups and application domains.

Our implementation is parameterized by the dimensions of the captured images as well as the size of interrogation windows and sub-areas. It is also parameterized by image quantization level (bits/pixel), the size of on-board memory and the overlap between interrogation windows. To the best of the authors’ knowledge, this is the first highly parameterized PIV system implemented on reconfigurable hardware. For a typical PIV configuration with images of 1024×1024 pixels, 40×40 pixel interrogation windows and 32×32 pixel sub-areas, we achieved a 100-fold speedup in hardware versus a standard software implementation.

High level PIV Architecture

Contributions

• A highly parameterized digital PIV system:
  • Designed using VHDL
  • Implemented on an FPGA board
• A library of parameterized VHDL components for digital PIV
• A C++ implementation of parameterized PIV

Examples

Measurement of the wake vortices of a lifting aircraft wing

Investigation of rotor aerodynamics with respect to noise emission of various noise sources such as blade/vortex interactions

Future work

Use FPGA implementation in a feedback loop to control a wing standing up in a water flow.

PIV Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th>Circuit1</th>
<th>Circuit2</th>
<th>Circuit3</th>
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<tbody>
<tr>
<td>Img_width</td>
<td>The width in pixels of the images</td>
<td>1024</td>
<td>1200</td>
<td>400</td>
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<td>Img_depth</td>
<td>The depth in pixels of the images</td>
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<td>Area_width</td>
<td>The width in pixels of the interrogation window</td>
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<td>40</td>
<td>50</td>
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<tr>
<td>Area_depth</td>
<td>The depth in pixels of the interrogation window</td>
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<td>40</td>
<td>50</td>
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<tr>
<td>Sub_area_width</td>
<td>The width in pixels of the sub-areas</td>
<td>32</td>
<td>32</td>
<td>20</td>
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<tr>
<td>Sub_area_depth</td>
<td>The depth in pixels of the sub-areas</td>
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<td>32</td>
<td>20</td>
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<tr>
<td>Displacement</td>
<td>Number of pixels by which a sub area is moved inside an interrogation window</td>
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<tr>
<td>Pixel_bits</td>
<td>Number of bits that represent a pixel</td>
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<tr>
<td>RAM_width</td>
<td>Number of bits in each memory address</td>
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<td>Overlap</td>
<td>Number of interrogation windows that overlap in an interrogation window size</td>
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Speedup of Different Circuits

<table>
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<th>Hardware latency</th>
<th>Software latency</th>
<th>speedup</th>
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<td>0.00473</td>
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Overview of the Strategic Research Plan

L3
PLUS

Bio-Med
S1
S2
S3

Enviro-Civil
S4
S5

L2
Validating TestBEDs

L1
Fundamental Science

R1
R2
R3